REMARKS

In response to the Office Action mailed March 30, 2004, Applicants amend their application and request reconsideration. In this Amendment, patented claims 8 and 9 and re-issue claims 17 and 18 are cancelled so that claims 1-7, and 10-16 remain pending.

Claims 9 and 18 were only objected to and those claims have been rewritten in independent form as amended claims 7 and 16, respectively, with the addition of certain previously omitted words. The added words are the same as those added to other claims as explained in the next paragraph. Thus, those claims are allowable and further comment on those claims is unnecessary.

In this Amendment the patented claims are clarified and the corresponding re-issue claims are similarly clarified. As to claims 2-6 and 11-15, inadvertent omissions are corrected merely to ensure that every claim term has proper antecedent basis. Articles are made uniform in use throughout the claims. These changes are made in order to make the claims more precise although there was no rejection of the claims as to form.

Patented claim 1 and re-issue claim 10 are similarly amended. In each claim the logic circuit is recited in a paragraph separate from the synchronous dynamic random access memory or the random access memory with the command decode system, in the case of claim 10, to make clear that the logic circuit is not part of the synchronous dynamic random access memory or the random access memory with a command decode system. Further, this format change makes apparent that the core cannot be considered part of the logic circuit but is part of the random access memory. While this distinction is clear in the patent, the formatting change in the two independent claims directed to apparatus removes any potential ambiguity in the claims.

The final paragraphs of each of claims 1 and 10 are similarly amended. These amendments make clear that the memory control circuit, which is clearly outside both the synchronous dynamic random access memory and the dynamic random access memory with a command decode system, outputs internal control signals. In other words, the internal control signals are generated outside the core unit and are supplied to the core unit from outside. This amendment further explains the arrangement illustrated in all of the embodiments of the invention depicted and described in the patent. For example, with respect to the embodiment of Figure 1, it is apparent that the internal control signals 112 and 114-118 are directly supplied to the core unit 104. By contrast, in the prior art structure illustrated in Figure 12 of the patent, as explained from column 1, line 65 to column 2, line 52, it is necessary to include a command decoder, not given a reference number in Figure

12, within the core unit 104. The command decoder is necessary because the signals supplied by controller 103 are not internal control signals, but rather only can become internal control signals by decoding. As explained in the patent, in the prior art the reason signals that are not internal control signals are supplied to the core unit is to avoid increasing the number of external terminals of the memory. As a result, there is a limitation to the operating speed of the memory. That limitation is overcome in the invention by producing the internal control signals in the memory control circuit and directly supplying those internal control signals to the core unit.

As already noted, claims 9 and 18 were only objected to and those claims are now presented in independent form as claims 7 and 16 so that those claims should be immediately allowed. The other claims remaining pending, claims 1-6 and 10-15 were rejected based upon the prior art described in the patent. Claims 1-6 were rejected as anticipated by the prior art description of the patent and claims 10-15 were rejected as unpatentable over the prior art described in the patent. These rejections are respectfully traversed and cannot be properly maintained based upon the clarifying amendments made here with respect to claims 1 and 10.

As already discussed, the prior art described with respect to Figure 12 of the patent does not disclose the generation of internal control signals outside the memory and the application of the internal control signals directly to the core unit of the memory. Thus, amended claim 1 cannot be anticipated by the prior art disclosure with respect to Figure 12 of the patent. For the same reason, amended claim 10 cannot be obvious over the prior art disclosure of the patent. It follows that the dependent claims depending from claims 1 and 10, namely claims 2-6 and 11-15, are patentable over that prior art disclosure for the same reason that their respective parent claims are patentable.

Reconsideration and allowance of all claims now pending is earnestly solicited.

Respectfully submitted,

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